REMARKS

Claims 1-21 are pending in the case. All claims stand rejected. In the present submission, claims 1-12 have been cancelled and claims 13-21 have been amended. Applicants have also amended the specification to remove the priority claim to an earlier filed application. Reconsideration is respectfully requested.

§102(e) Rejections

Claims 1, 5, 9, 13, 14 and 18 have been rejected under 35 U.S.C. §102(e) as being anticipated by Hsieh et al. (US 6,757,019). Applicant respectfully traverses the rejection.

In the present submission, claims 1, 5 and 9 have been cancelled and therefore the rejection as to these claims is now moot.

Claim 13

Regarding Claim 13, the Examiner contends that Hsieh discloses every element of the claim including a "dual-port data memory." Applicant respectfully submits that Hsieh in fact does not disclose a "dual-port data memory." A "dual-port data memory" is a well-known term of art and refers to a memory including two ports, each port having separate address, data and control signals for accessing a common memory array. Applicant submits herewith an application note from IDT entitled "Introduction to Multi-Port Memories" (2 pages) and an application note from Dallas Semiconductor entitled "Dual Port RAM" (6 pages) for the Examiner's reference. The two application notes describe the structure and explaining the operation of a dual port memory as is well known by one of ordinary skill in the art.

Claim 13 is therefore patentable over Hsieh at least by reciting "a dual-port data memory, a first port of said dual-port data memory coupled to said sensor array for storing said pixel data, and a second port of said dual-port data memory providing a memory interface for exporting said pixel data."

Claim 14

Regarding Claim 14, the Examiner contends that Hsieh discloses every limitation of the claim. In the present amendment, Claim 14 has been amended to clarify that the image processing device is formed on an integrated circuit separate from the image sensor and that

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the logic circuit provides a memory interface protocol for exporting the pixel data between the image sensor and the image processing device.

Specifically, Claim 14, as amended, recites:

> 14. An imaging system, comprising:
> an image sensor, comprising:
> a sensor array, including a two-dimensional array of pixel elements, that outputs digital signals as pixel data representing an image of a scene;
> a data memory coupled to said sensor array and fabricated with said sensor array on a first integrated circuit, said data memory for storing said pixel data, wherein said data memory is configured using a first memory interface protocol;
> a logic circuit coupled to said data memory and fabricated with said data memory on said first integrated circuit, **said logic circuit for accessing said data memory using said first memory interface protocol and performing memory interface conversion to provide an output memory interface configured using a second memory interface protocol** different than said first memory interface protocol **for exporting said pixel data out of said first integrated circuit**; and
> **an image processing device formed on a second integrated circuit** separate from said first integrated circuit and **including a memory interface port configured using said second memory interface protocol**;
> wherein said image sensor is coupled to said memory interface port of said image processing device and said image processing device accesses pixel data in said image sensor using said second memory interface protocol. (Emphasis added.)

Claim 14, as amended, is patentable over Hsieh at least by reciting "an image processing device formed on a second integrated circuit separate from said first integrated circuit and including a memory interface port configured using said second memory interface protocol." In Hsieh, the photosensor and the processor array are formed on a "single monolithic integrated circuit chip" (See Abstract of Hsieh). When the processor array is formed on the same integrated circuit as the photosensor, the processor array does not require a "memory interface port" for accessing the pixel data in the image sensor. To the contrary, Claim 14 recites forming an imaging system where the image sensor and the image processing device are formed on separate integrated circuits and the image processing device includes a memory interface port employing a memory interface protocol to access the pixel data from the image sensor. Claim 14 is therefore patentable over the cited reference.

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Claim 18

Regarding Claim 18, the Examiner contends that Hsieh discloses every limitation of the claim. In the present amendment, Claim 18 has been amended to clarify that the image processing device is formed on an integrated circuit separate from the image sensor and that the logic circuit provides a memory interface protocol for exporting the pixel data between the image sensor and the image processing device.

Specifically, Claim 18, as amended, recites:

> 18. A method in an image sensor, comprising:
> capturing an image of a scene using a sensor array;
> storing pixel data representative of said images in a data memory being fabricated on a same integrated circuit as said sensor array, wherein said data memory is configured using a first memory interface protocol;
> **outputting said pixel data to an image processing device outside of said integrated circuit using a second memory interface protocol; and**
> **receiving said pixel data at said image processing device using said second memory interface protocol, said image processing device being formed on an integrated circuit separate from the integrated circuit on which the sensor array and data memory are formed.** (Emphasis added.)

Claim 18, as amended, is patentable over Hsieh at least by reciting "receiving said pixel data at said image processing device using said second memory interface protocol, said image processing device being formed on an integrated circuit separate from the integrated circuit on which the sensor array and data memory are formed." As discussed above with reference to claim 14, Hsieh describes a single-chip photo-sensor/processor array system. Hsieh does not teach or suggest receiving the pixel data at an image processing device that is formed on a separate integrated circuit as the image sensor integrated circuit, as recited in Claim 18.

§103(a) Rejection

Claims 2-4, 6-8, 10-12, 15-17 and 19-21 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh in view of Shepherd et al. (U.S. 6,434,665). Applicant respectfully traverses the rejection.

In the present submission, claims 2-4, 6-8 and 10-12 have been cancelled and therefore the rejection as to these claims is now moot.

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Claims 15-17

Claims 15-17, dependent upon claim 14, are patentable over Hsieh at least for the same reason that claim 14 is patentable. Shepherd does not cure the deficiency of Hsieh. Therefore, claims 15-17 are patentable over the cited references.

Claims 19-21

Claims 19-21, dependent upon claim 18, are patentable over Hsieh at least for the same reason that claim 18 is patentable. Shepherd does not cure the deficiency of Hsieh. Therefore, claims 19-21 are patentable over the cited references.

CONCLUSION

Claims 1-21 are pending in the present application. In the present submission, claims 1-12 have been canceled and claims 13-21 have been amended. For the above reasons, claims 13-21 are in condition for allowance. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

Certification of Facsimile Transmission

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature — November 12, 2004 (Date)

Respectfully submitted,

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INTRODUCTION TO MULTI-PORT MEMORIES

APPLICATION NOTE AN-253

By Cheryl Brennan

What is a multi-port SRAM?

A multi-port is a static RAM with a dual-port or multi-port cell. Each port has separate address, data and control signals for accessing a common SRAM array.

How many transistors does each cell have?

IDT dual-ports typically use six transistors and two resistors per cell. Figure 1 depicts IDT's standard SRAM cell. It is a four transistor cell with high impedance pull-up resistors to provide the proper circuit biasing. Figure 2 depicts the configuration of IDT's dual-port SRAM cell. This can be described as a standard four transistor memory cell with two additional transistors to provide an additional access path to the cell for both ports.

Figure 3 shows the configuration of IDT's FourPort SRAM cell. There are an additional four transistors. This allows up to four devices to access the memory simultaneously.

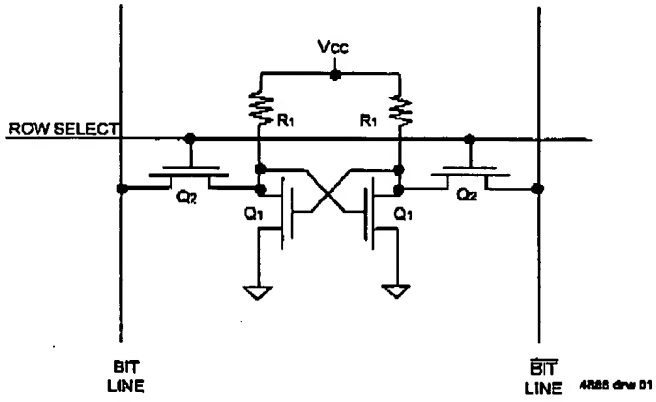

Figure 1. Standard Four Transistor Two Resistor Memory Cell

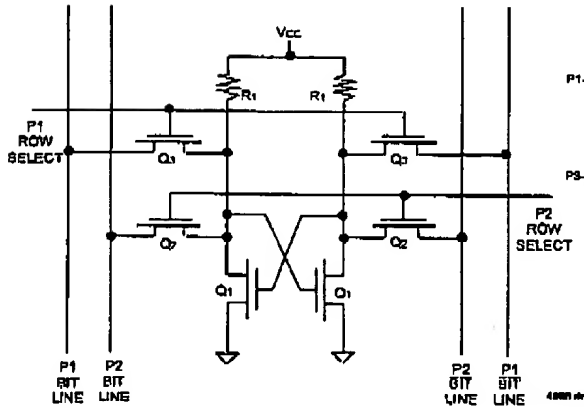

Figure 2. Dual-Port Memory Cell

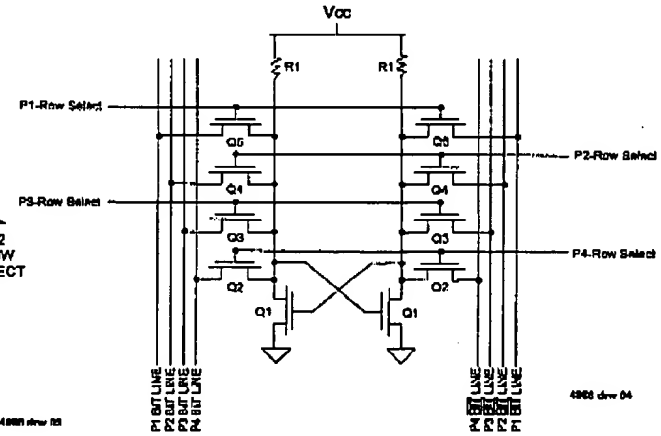

Figure 3. A Simple Example of a FourPort™ SRAM Configuration.

MARCH 2000

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What are the different types of multi-port memories available?

- Asynchronous Dual-port SRAMs
- Synchronous Dual-port SRAMs
- FourPort™ SRAMS
- SARAM™ (Sequential Access Random Access Memory)
- Bank-Switchable™ Dual-port SRAMs

What are the differences between these various Multi-Port memories?

Asynchronous Dual-ports SRAMs—These dual-ports respond to address and control pin changes without the need for clocks or counters. These devices allow simultaneous access to a single static SRAM memory location from two busses. Refer to Application Note AN-91, "The Most Commonly Asked Questions About Asynchronous Dual-Ports." Most asynchronous dual-ports have arbitration logic.

Synchronous Dual-ports SRAMs—As the need for bandwidth has increased, there became a greater demand for faster internal operating speeds in dual-ports. The solution was introduced by IDT in 1992. The synchronous Dual-Ports use external clocking and internal counters to allow designers to run at faster speeds than that which can be achieved from standard asynchronous dual-ports. These dual-ports respond synchronously to address and control pin changes in relation to a clock edge. These devices allow simultaneous access to the same location in memory. IDT has two different options available on most synchronous dual-ports, Pipelined and Flow-through. The Pipelined option provides the highest bandwidth. The Flow-through synchronous option is used by designers who want the ease of integrating a synchronous dual-port in their synchronous system design. Additionally, we offer two different pinout architectures of the IDT synchronous dual-ports. In 1999 IDT introduced a 133MHz synchronous dual-port. In order to achieve the 133MHz performance it was necessary to interleave the I/O pins. For more information on the issues above refer to Application Note AN-254, "The Most Commonly Asked Questions About Synchronous Dual-Ports."

FourPort™ SRAMs—These devices need similar to the standard Asynchronous Dual-Ports. These devices allow simultaneous access to a single static SRAM from up to four processors. There are no clocks or counters needed. Most asynchronous dual-ports have arbitration logic. Refer to Application Note AN-91, The Most Commonly Asked Questions About Asynchronous Dual-ports.

SARAM™—The SARAM™ is a Sequential Access Random Access Memory. This device that allows the designer to bridge the asynchronous and synchronous components of a system design. The SARAM™ has a sequential FIFO-like interface on one side and a SRAM on the other side. Refer to Application Note AN-120, "Functional Description of the IDT70825 SARAM™."

Bank-Switchable™ Dual-Port SRAM—The difference between a Dual-Port SRAM and the Bank Switchable Dual-Port SRAM is the number of transistors used in the cell. The Bank Switchable Dual Port uses the standard four transistor memory cell (see Figure 1). The BSDP is divided into four banks of memory. The Bank Switchable Dual-Port allows simultaneous access to the memory array, but each of the four banks can be accessed from only one port at a time.

What application notes are available?

- AN-02—Dual-port Simplify Communications in Computer Systems
- AN-09—Dual-port SRAMs Yield Bit Slice Designs Without Microcode
- AN-14—Dual-port SRAMs with Semaphore Arbitration
- AN-42—Using the IDT7050/7052 FourPort™ SRAMs in DSP and Matrix Processing Applications
- AN-43—The IDT FourPort™ SRAM Facilitates Multiprocessor Designs
- AN-45—Introduction to IDT's FourPort™ SRAM
- AN-59—Using IDT7024 and IDT7025 Dual-Port Static RAMs to Match System Bus Widths
- AN-68—Dual-port SRAM Simplifies PC-to-TMS320 Interface
- AN-70—Dual-port Interrupt Expansion
- AN-91—The Most Commonly Asked Questions About Asynchronous Dual-ports
- AN-120—Functional Description of the IDT70825 SARAM™
- AN-144—Synchronous Dual-Port Static RAMs for DSP and Communication Applications
- AN-253—Introduction to Multi-Port Memories
- AN-254—The Most Commonly Asked Questions About Synchronous Dual-ports
- AN-255—Dual-port Power and Board Layout Discussion

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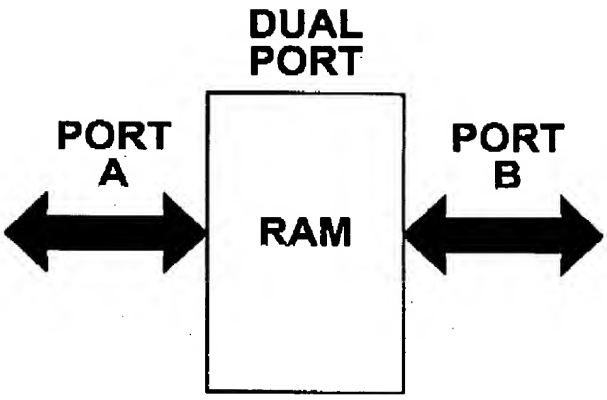
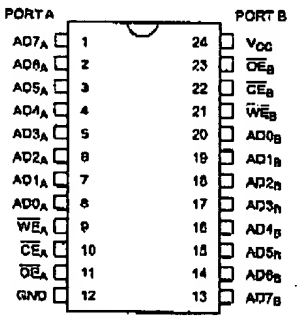
DALLAS SEMICONDUCTOR

Application Note 62
Dual Port RAM

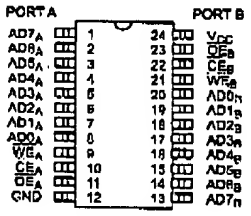


Memory devices and systems are diversifying and becoming more complex out of necessity to support information processing needs. The need to centralize data storage in multiprocessor applications challenges both hardware and software designers. New ways must be found that consolidate system information that is controllable by more than one bus. In addition, systems are becoming more power conscious, particularly portable systems as they typically rely on some kind of rechargeable battery for power. For systems where shared bus access requirements are infrequent, but require many megabytes of memory to be transferred, a shared mass storage device such as a floppy disk drive or networked hard disk drive may suffice. However, for frequent, low density access, media such as hard drives or floppy diskettes are impractical and would greatly slow the rate at which data could be stored and retrieved. The DS1609 Dual Port Ram has been specifically designed to be able to meet high frequency, low volume data storage and retrieval between two asynchronous systems. With its ability to operate at voltages as low as 2.5 volts, the DS1609 also fits easily into any portable application where power availability is limited.

PIN ASSIGNMENT



DS1609
24 PIN DIP (600 mil)



DS1609S
24 PIN SOIC (300 mil)

PIN DESCRIPTION

V_{CC}	+5 VOLT SUPPLY
GND	GROUND
AD0–AD7	PORT ADDRESS/DATA
$\overline{CE}$	PORT ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE

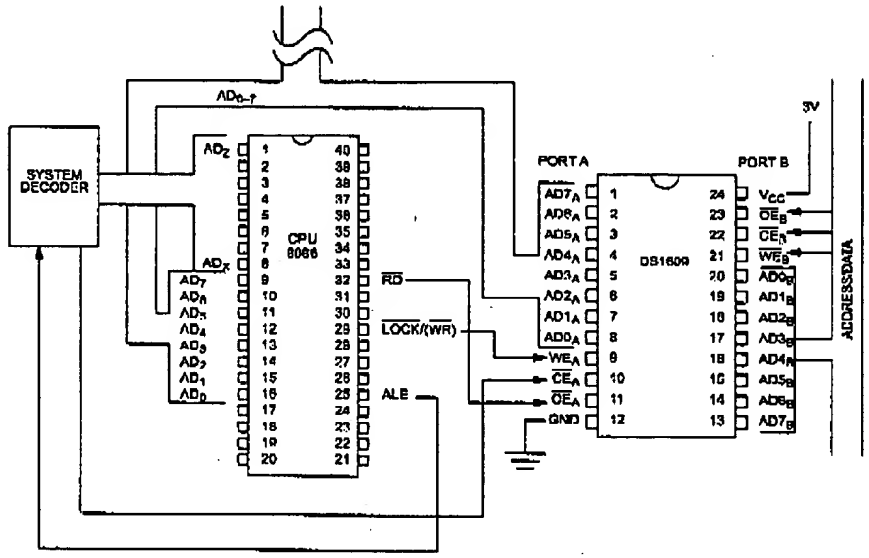
The type of bus which may be connected to either port of the DS1609 is not limited to system level. A multiplexed microprocessor address and data bus can be connected directly to either or both ports of the DS1609. The device can be controlled from either bus port separately by only three signals, $\overline{OE}$, $\overline{CE}$, and $\overline{WE}$. The obvious disadvantage of the multiplexed bus is the slightly reduced system performance because address and data information is being transmitted serially. The equally obvious advantage is the reduced pin count achievable by multiplexing the addressing and data buses.

Read/Write access of either port is transferred as 8 bits address, followed by 8 bits of data. In a read cycle to a port, $\overline{WE}$ is inactive, and the cycle is initiated when $\overline{CE}$ goes active, which with the address latched, data is retrieved under the control of $\overline{OE}$. The rising edge of either $\overline{CE}$ or $\overline{OE}$ terminates the read cycle. For a write cycle, $\overline{OE}$ is inactive, and $\overline{CE}$ becoming active latches the address to be accessed, with $\overline{WE}$ becoming active.

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports. Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or a write from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write contention does not occur is to perform redundant read cycles. Write/write contention needs can be avoided by assigning groups of addresses for

write operations to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

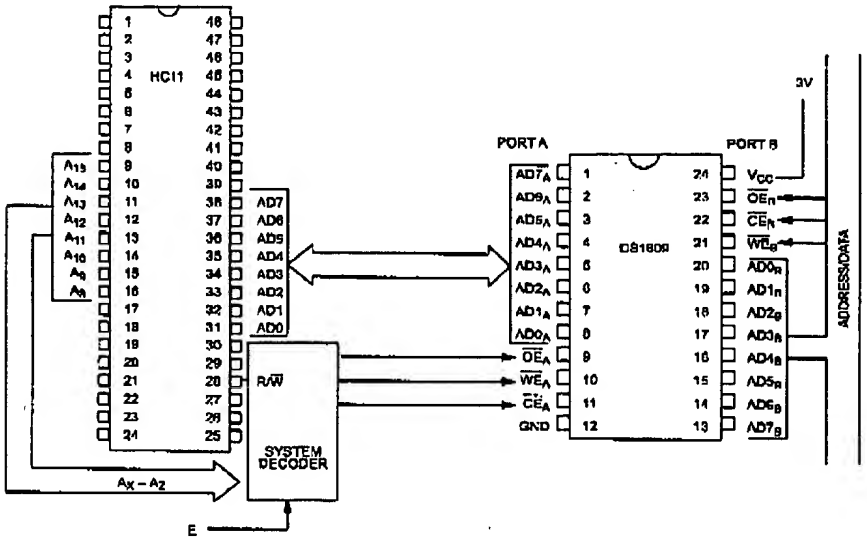
DS1609 DUAL PORT INTERFACE TO INTEL 8086 MICROPROCESSOR Figure 1



The DS1609 is ideally suited for small microprocessor based systems which frequently utilize dedicated 8 bit multiplexed address/data busses the following examples deal with interfacing with the Intel 8086/8088 series and the Motorola HC11 series microprocessors.

For implementation with the Intel 8086/8088 microprocessor family, the address/data pins of either port may be tied directly to the lower 8 address data lines of the Intel 8086 or 8088 microprocessor (Figure 1). The $\overline{RD}$ pin from the microprocessor provides the $\overline{OE}$ input to the port on the DS1609, while $\overline{WR}$ provides the $\overline{WE}$ input to the port. The port's $\overline{CE}$ input may be conditioned by a system decoder, which would require the 8086's ALE output as an input to provide address latching. Several of the unused address/data lines from the 8086 would also be required as inputs to indicate where the DS1609 resides in the system memory map. In applications where multiple DS1609 ports are required, multiple $\overline{CE}$ outputs could be provided from a system decoder using the ALE signal from an Intel 8086/8088 with user specified address lines to generate multiple chip selects (Figure 3).

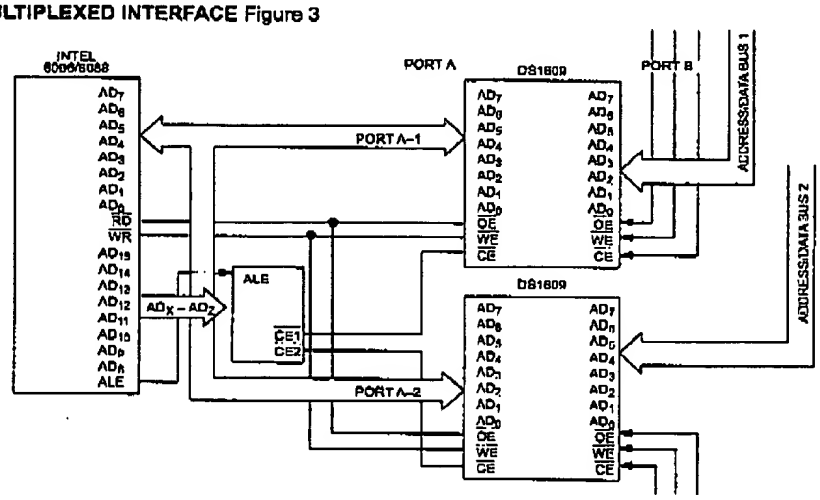
MOTOROLA HC11 EXPANDED MODE Figure 2



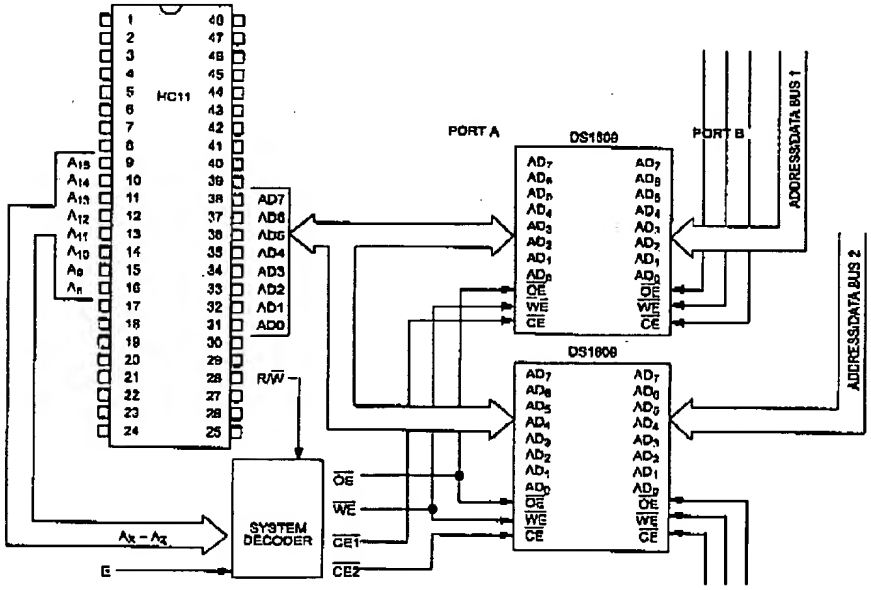
For implementation with the Motorola HC11 microprocessor family, the address/data pins of either port on a DS1609 may be directly tied to port C of an HC11 operating in expanded mode (Figure 2). Address pins from port B of the HC11 ($A_8 - A_{15}$) may be used to provide the DS1609's location in the system memory map. The E signal, which is also an input to the HC11, provides a bus clock to the system decoder indicating whether the HC11 is in an address or data cycle. The R/$\overline{W}$ input to the decoder indicates whether the HC11 is writing or reading data in a data cycle. From these inputs, a system decoder can provide $\overline{OE}$, $\overline{WE}$, and $\overline{CE}$ outputs to DS1609. For applications where more density is required, two DS1609's may be used. The same inputs, including a user selected combination of address lines $A_8 - A_{15}$ can be used to provide $\overline{OE}$, $\overline{WE}$, and multiple $\overline{CE}$ signals for individual DS1609 devices (Figure 4).

The DS1609 may be used with other microprocessors without multiplexed busses, which have a separate address and data bus.

MULTIPLEXED INTERFACE Figure 3

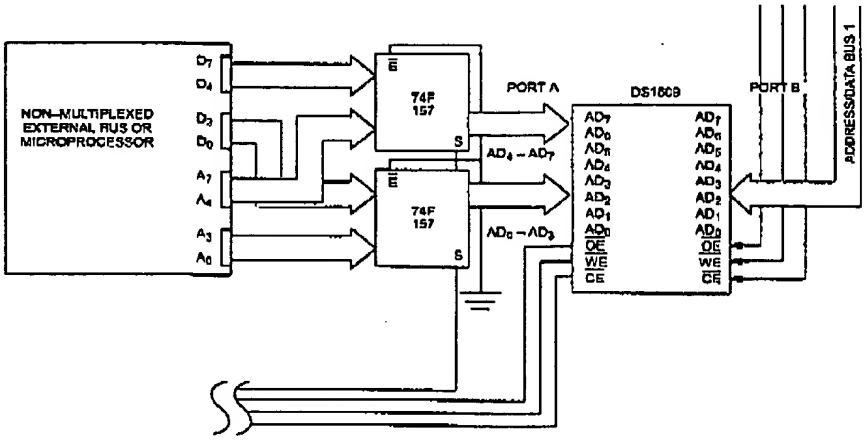


MOTOROLA HC11 EXPANDED MODE MULTIPLE DS1609'S Figure 4



The DS1609 can be used as a go between with non-multiplexed microprocessors such as the Intel 386 or Motorola 68030. Processor cycles to and from a DS1609 must then be multiplexed specifically for the DS1609's address/data/bus. An example implementation is shown below (Figure 5).

SAMPLE IMPLEMENTATION; NON-MULTIPLEXED BUS Figure 5



In this implementation, the lower 8 bits of a microprocessor's address bus and data bus are connected to the multiplexed address and data inputs using two 74F157 quad 2 input multiplexers. Each of the 74F157 devices takes 4 address and 4 data inputs originating from a microprocessor or an external bus master. The 74F157s produce four outputs of multiplexed address/data information which can then be used by a DS1609 port. The $\overline{E}$ inputs of each 74F157 may be tied to ground. The S inputs on the 74F157's become control logic, and direct switching back and forth between passing the address lines or the data lines. Read and write enabling signals must be provided by the microprocessor or external bus master.

IN SUMMARY

The DS1609 Dual Port RAM is tailored for use with 8 bit multiplexed address/data bus microprocessors. The DS1609's unique asynchronous dual port access allows a system design to provide a 256 bytewide registers which may be shared by two independent microprocessors. Multiple DS1609's may be tied together in a system to provide for 3 microprocessors having access to two 256 byte memories. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while providing for the unique asynchronous access. For systems which do not have a multiplexed address/data bus, minimal logic can convert separate address and data lines into a multiplexed address/data bus usable by the DS1609.